

Replacement Sheets

Drawings

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Applicant : IOAN DANCEA

Application/Control No. : 09/874,027

Title : METHOD AND VLSI CIRCUITS ALLOWING TO CHANGE
DYNAMICALLY THE LOGICAL BEHAVIOUR

EXAMINER : FRED FERRIS, Patent Examiner
Simulation and Emulation, Art Unit 2128

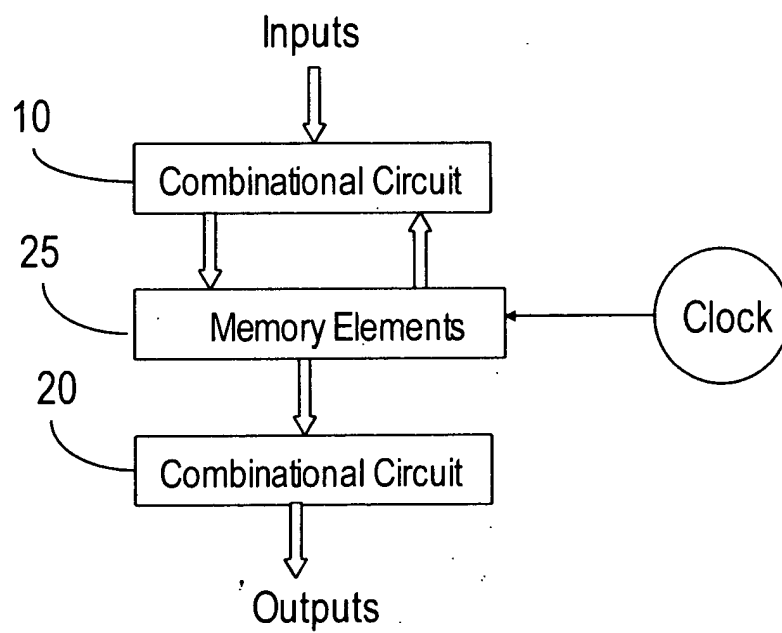


FIGURE 1
(Prior Art)

Replacement Sheet

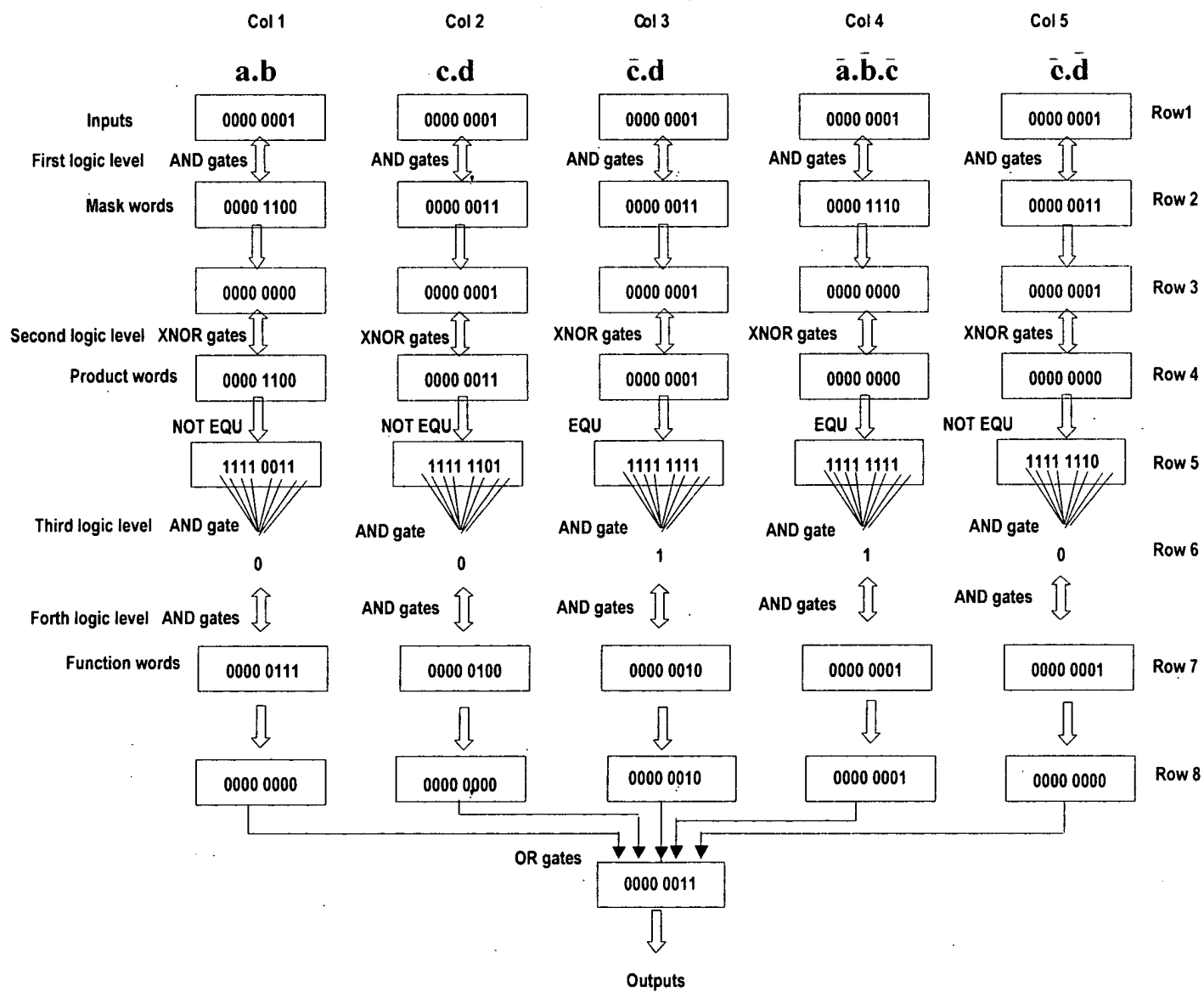


FIGURE 2A

Replacement Sheet

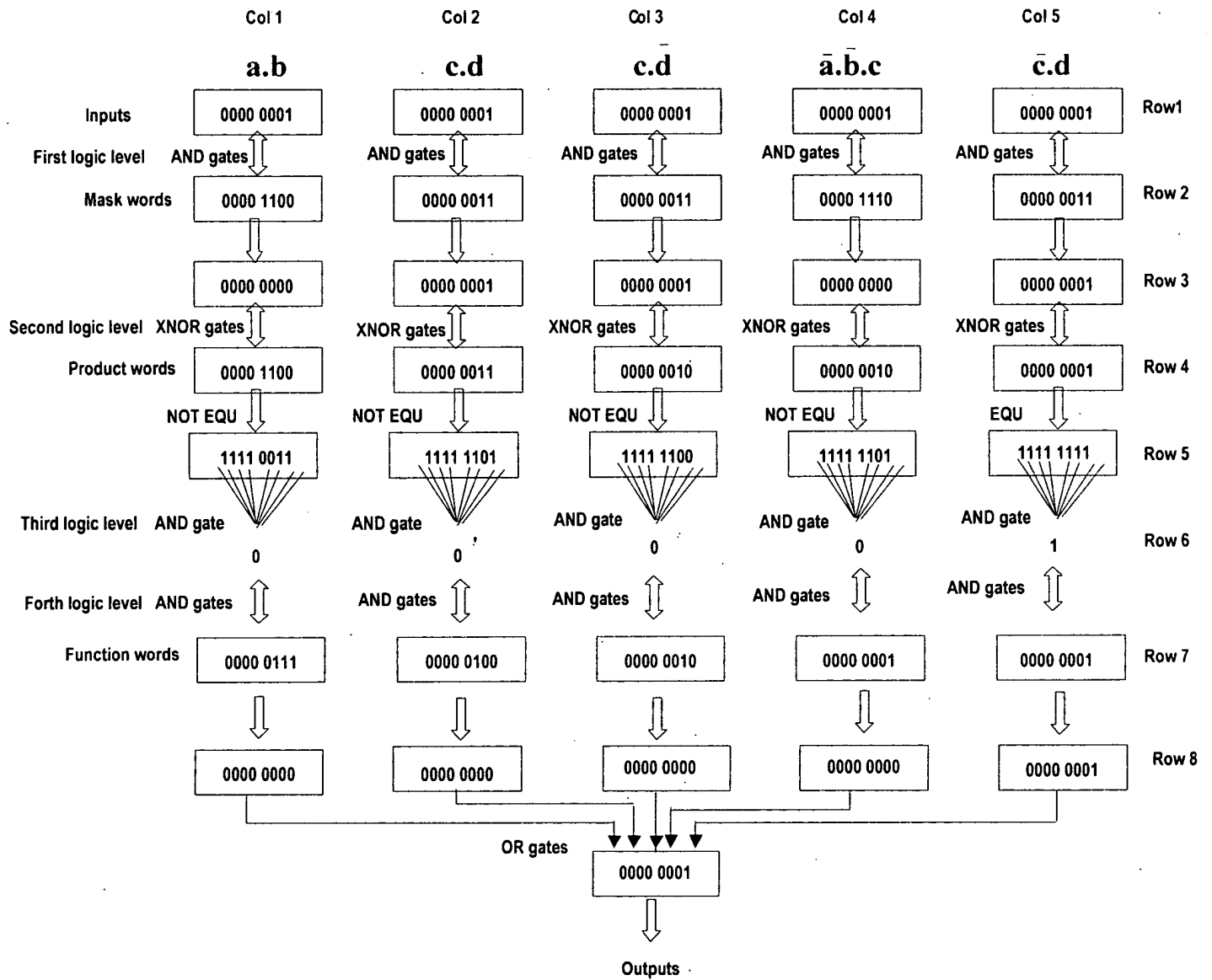


FIGURE 2B

Replacement Sheet

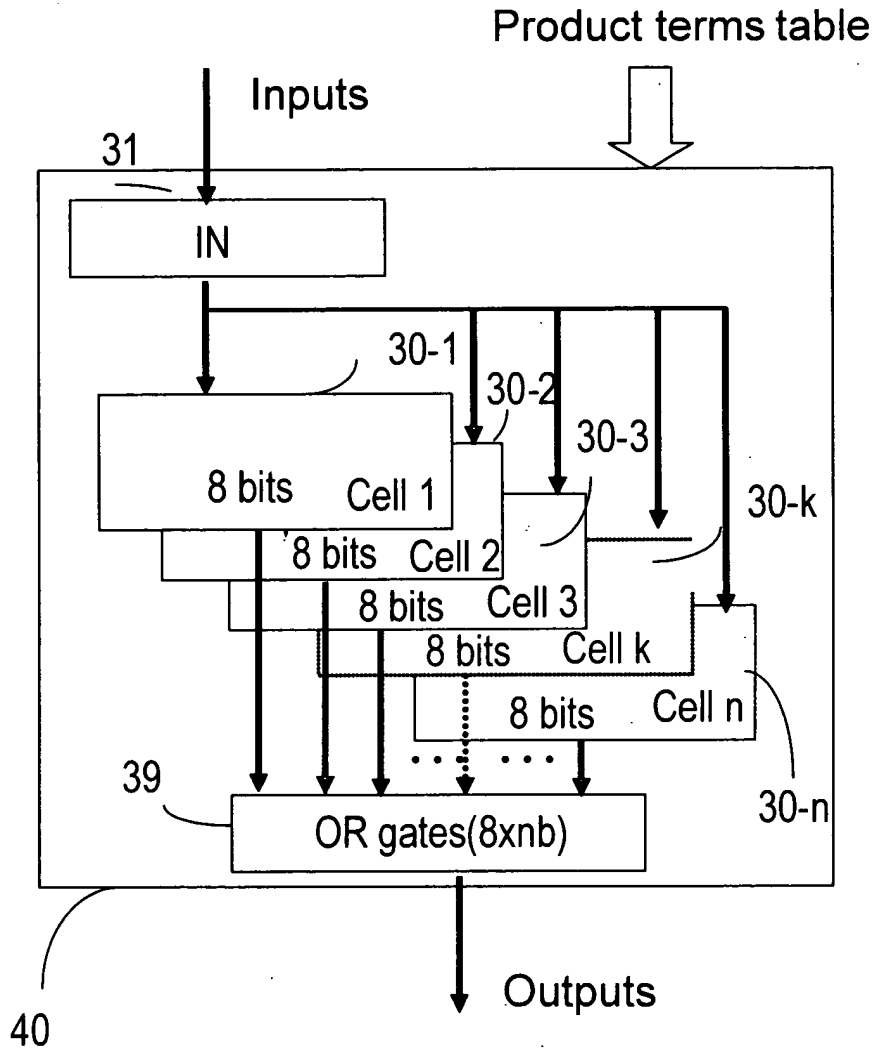


FIGURE 3

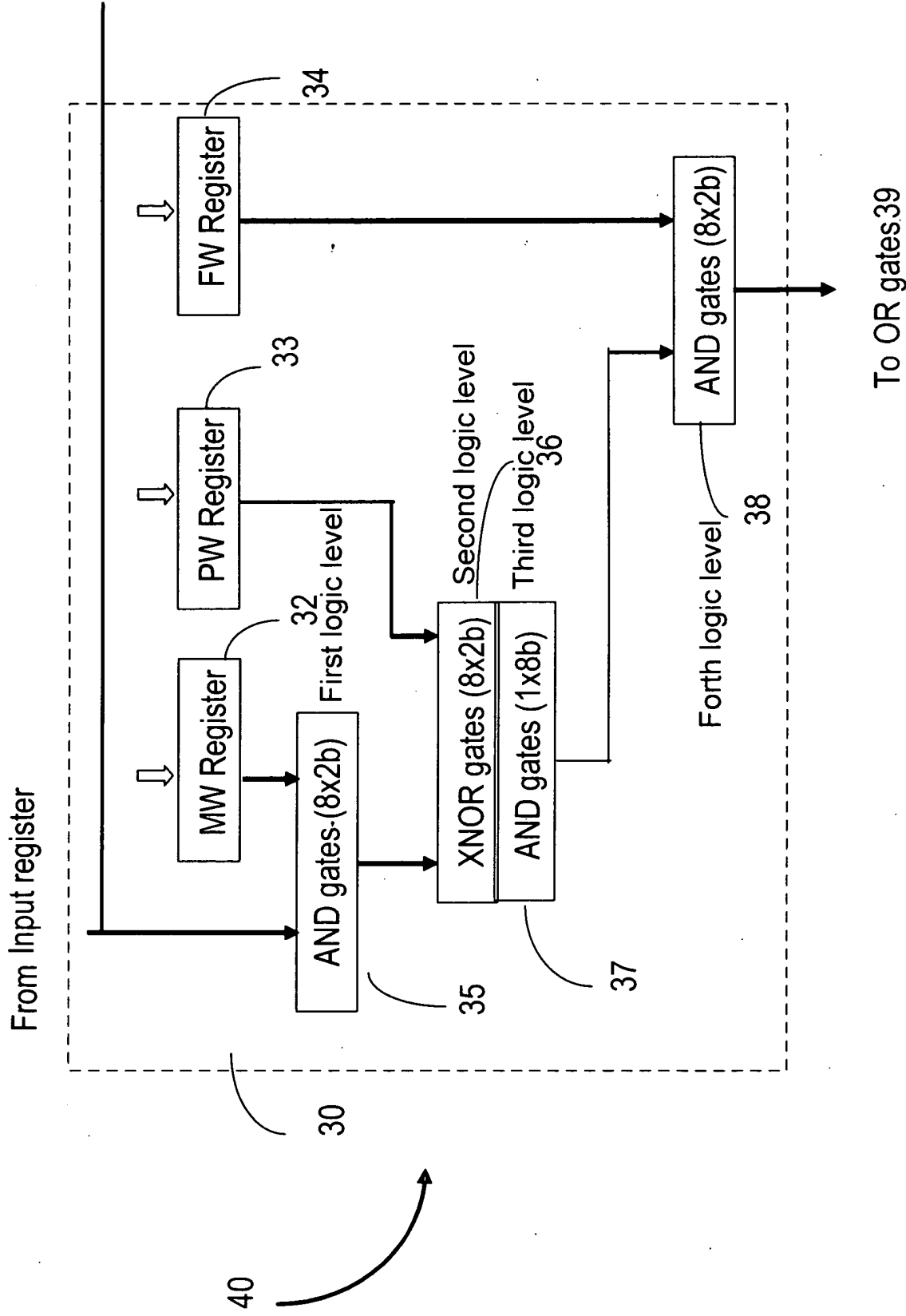


FIGURE 4

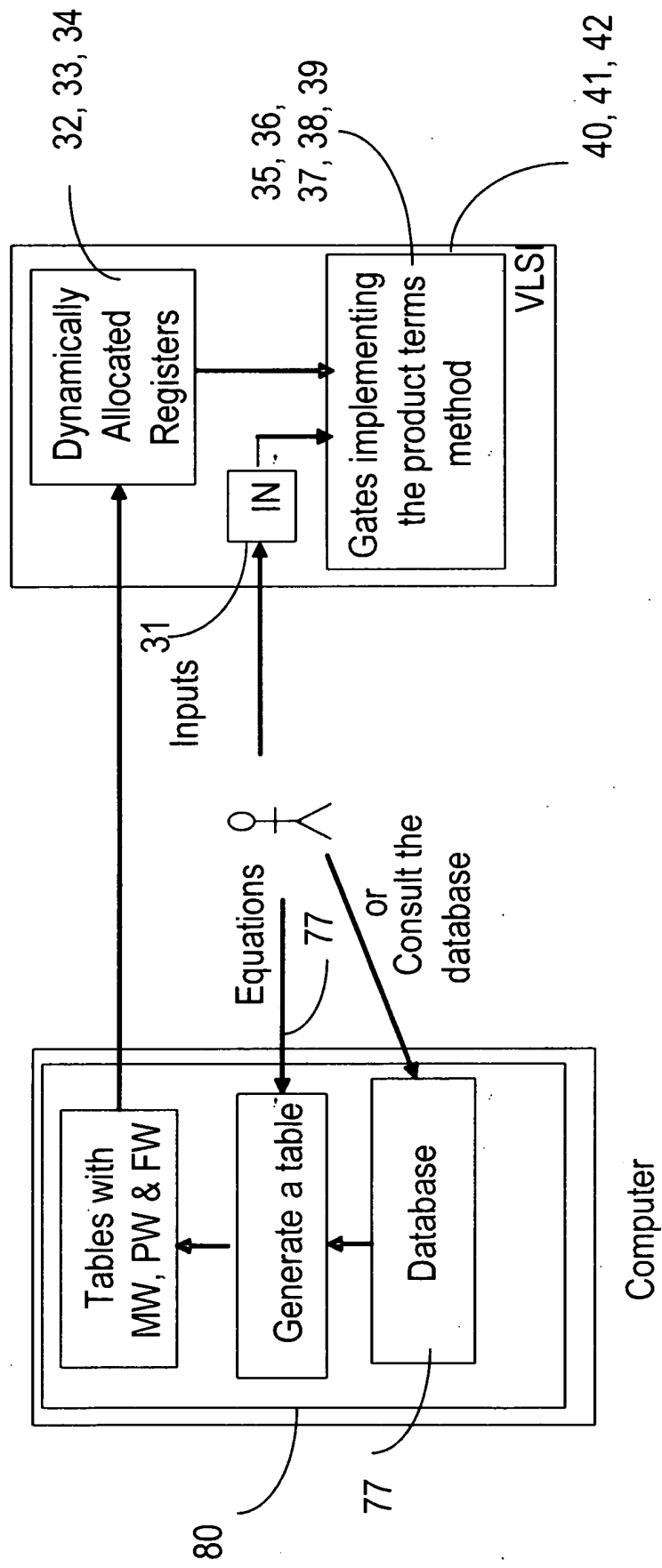


FIGURE 5

Product terms table

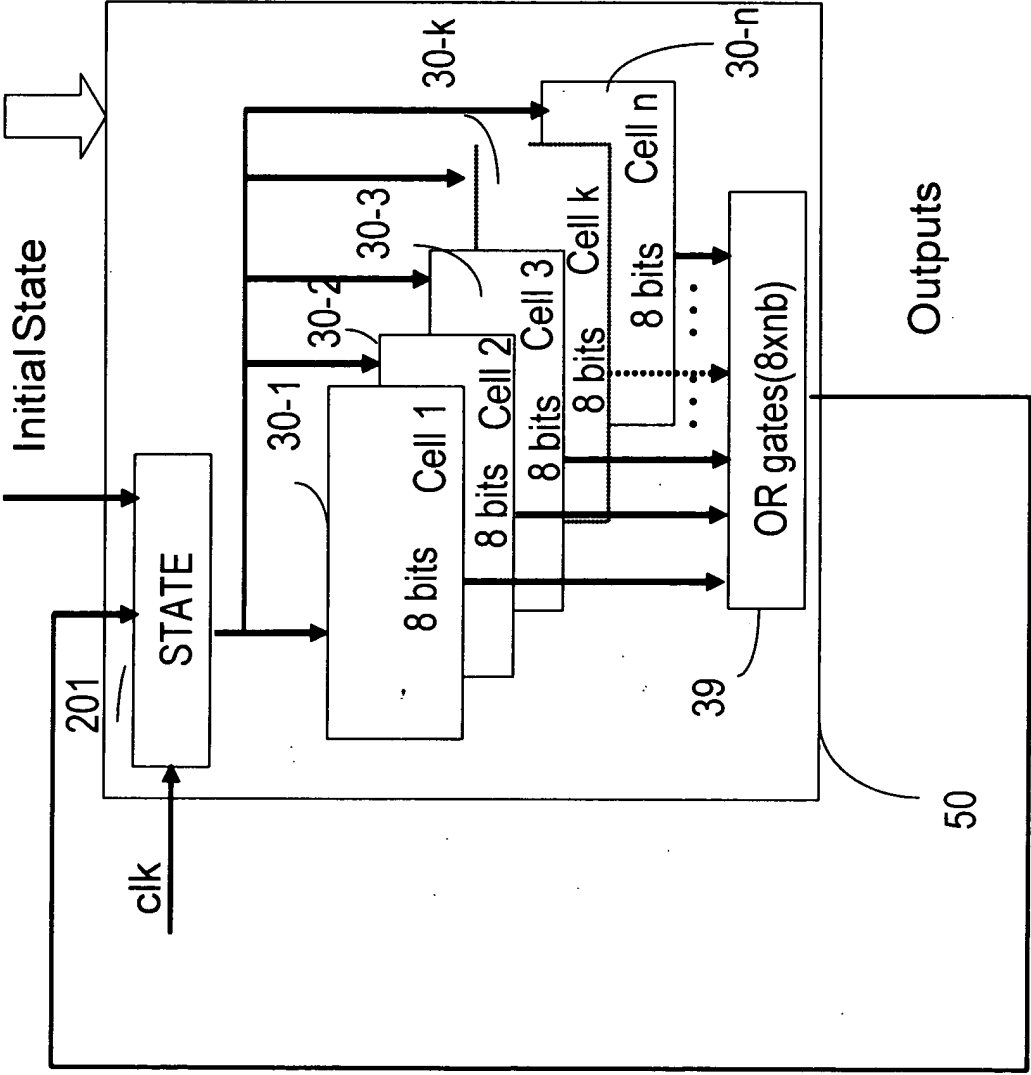
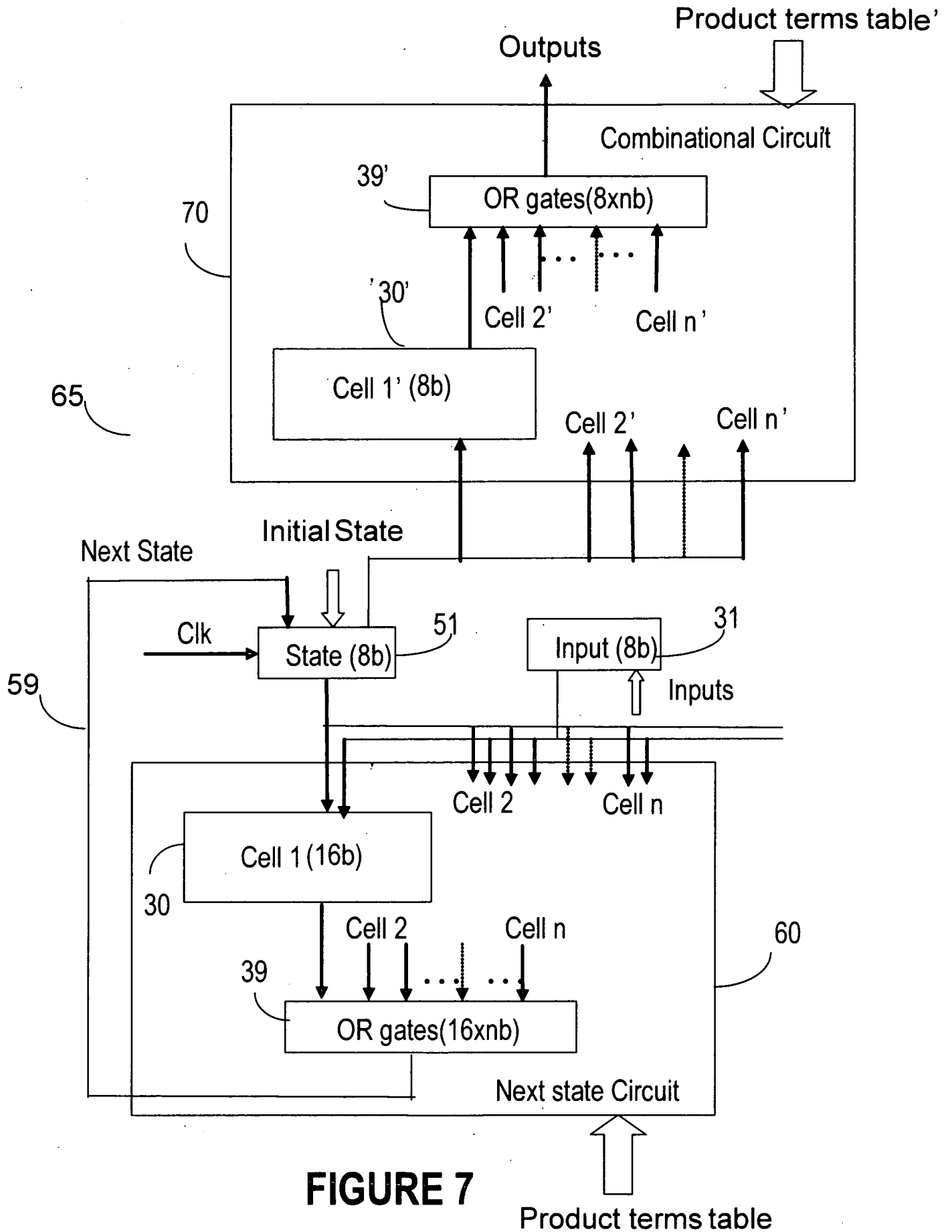


FIGURE 6

Replacement Sheet



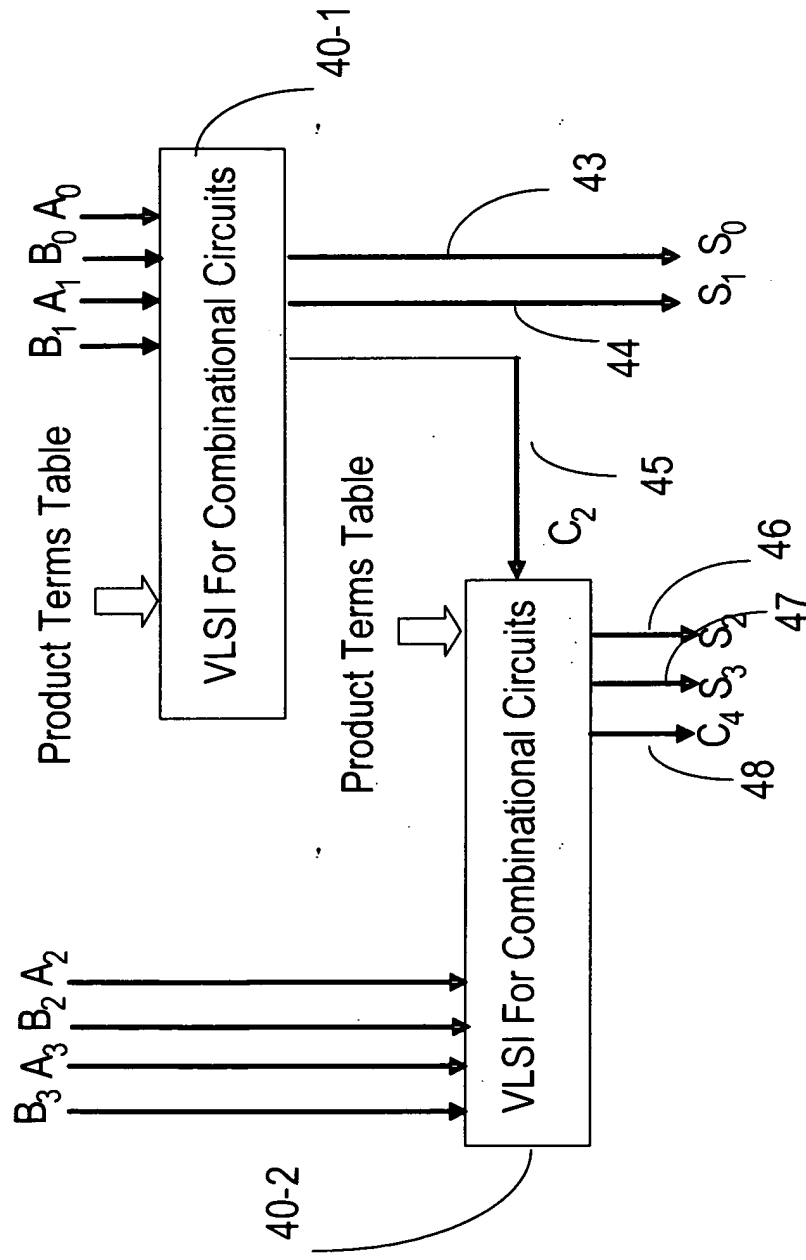


FIGURE 8

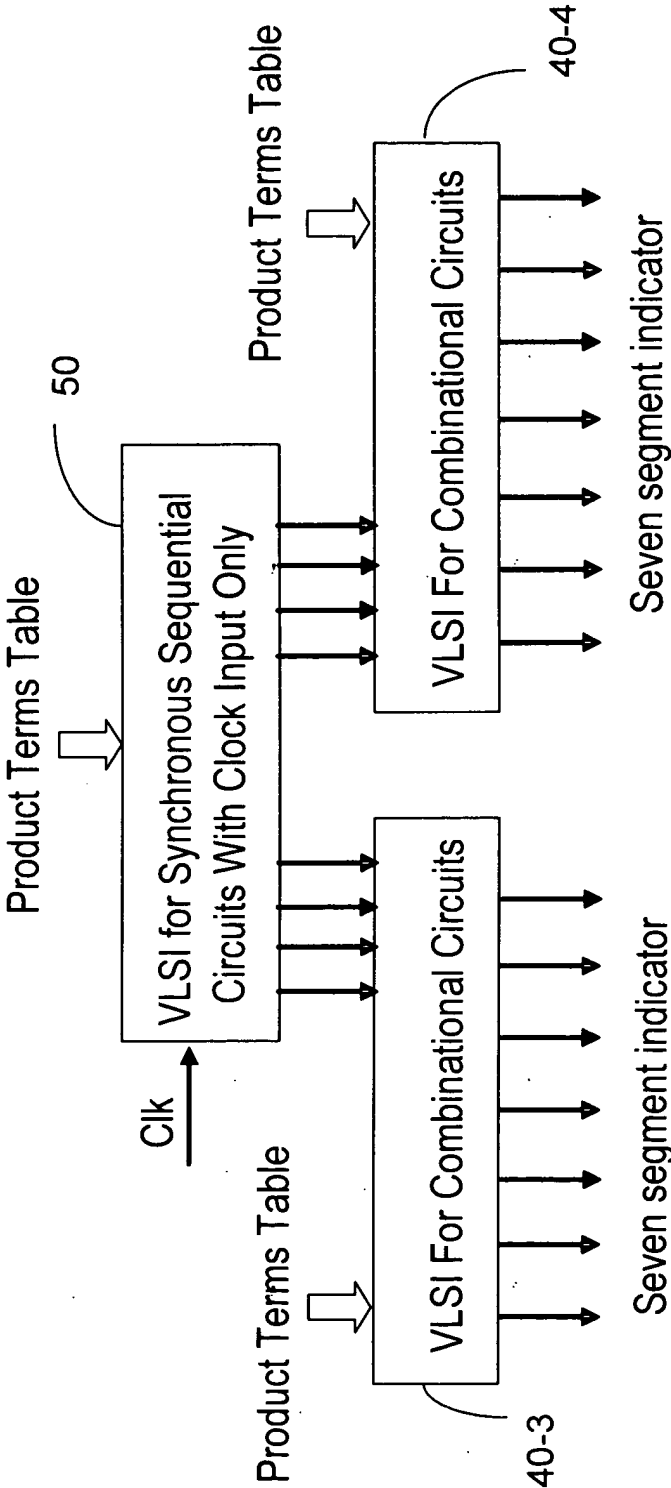


FIGURE 9

Replacement Sheet

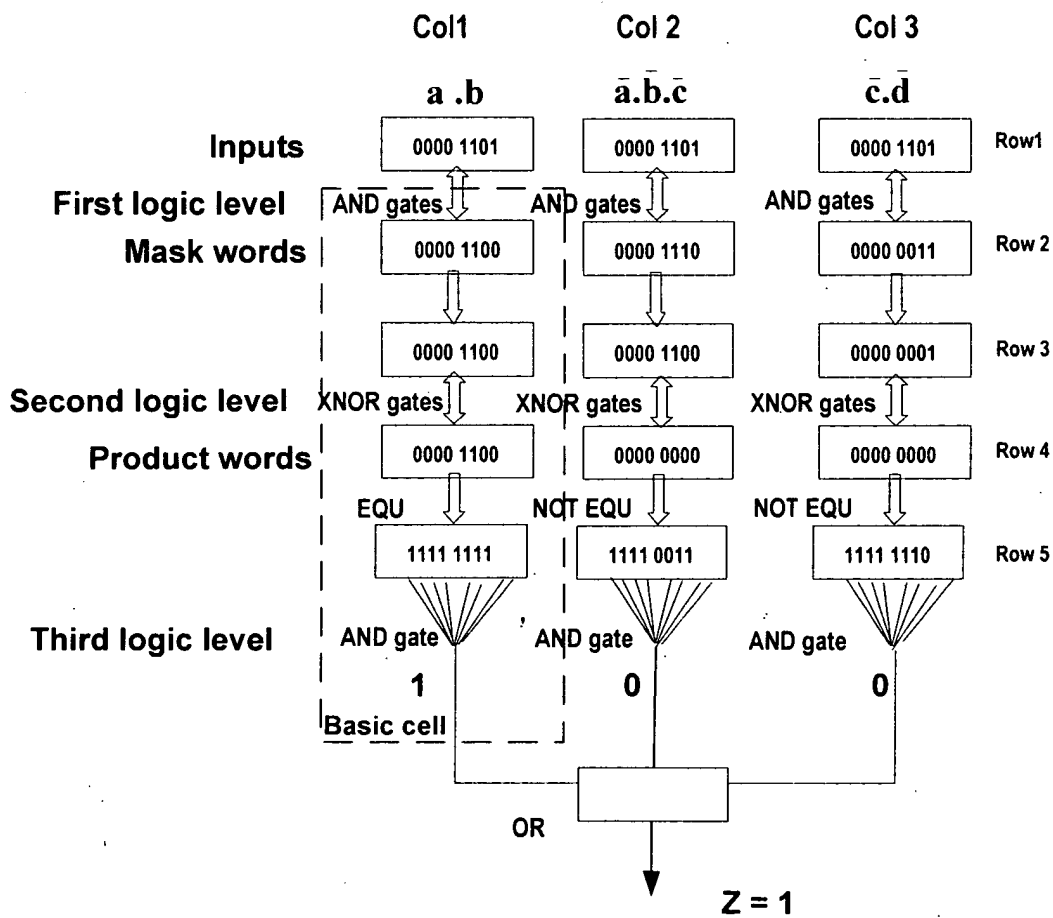


FIGURE 10

Replacement Sheet

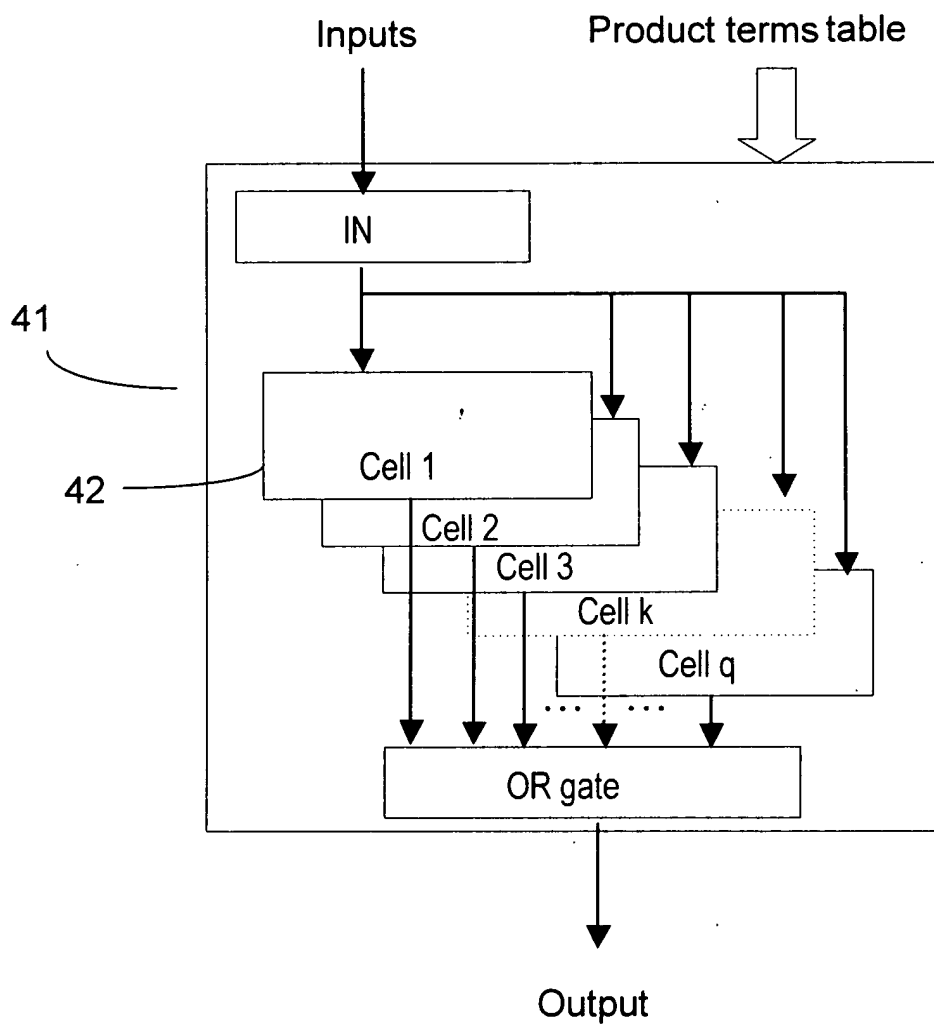


FIGURE 11

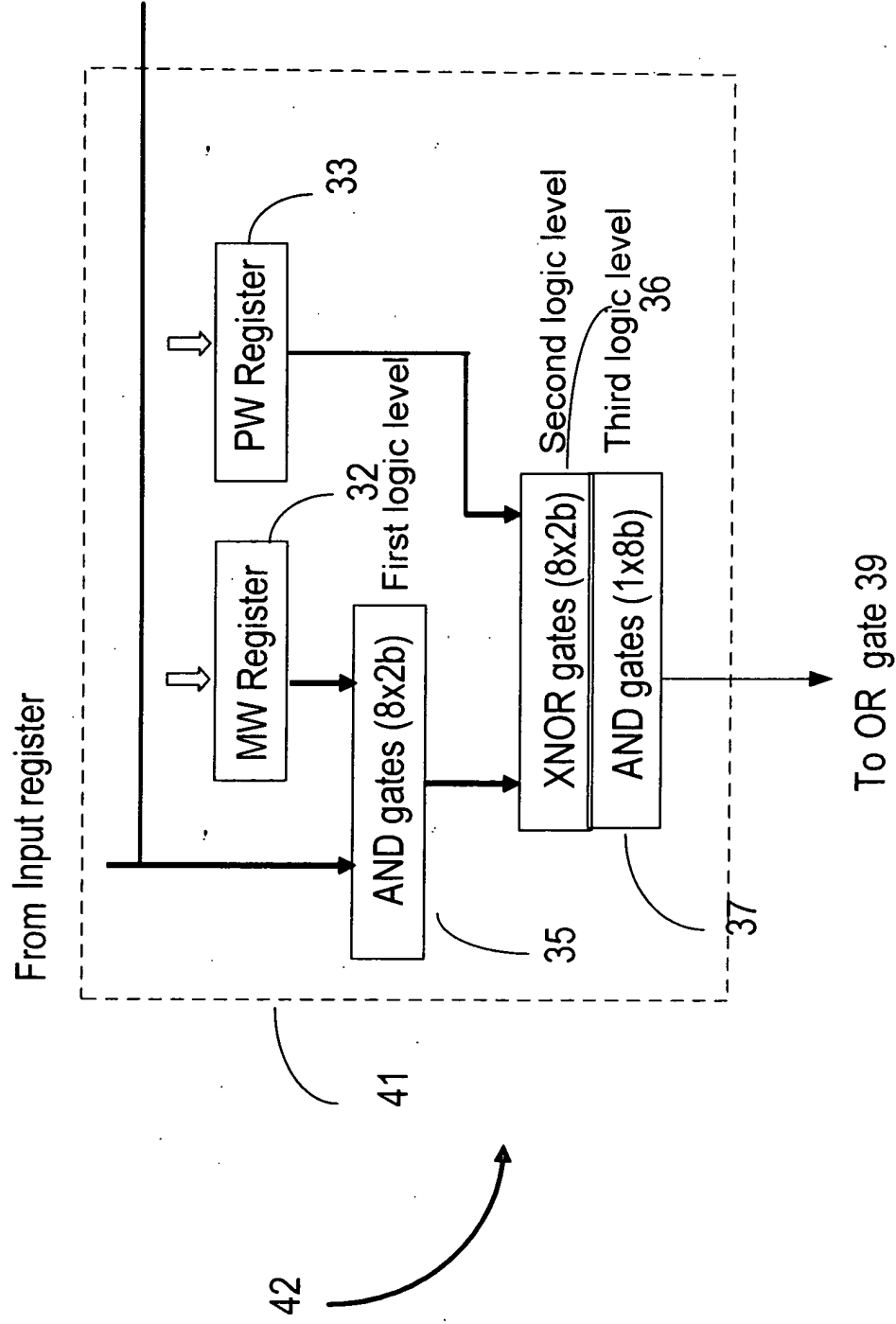
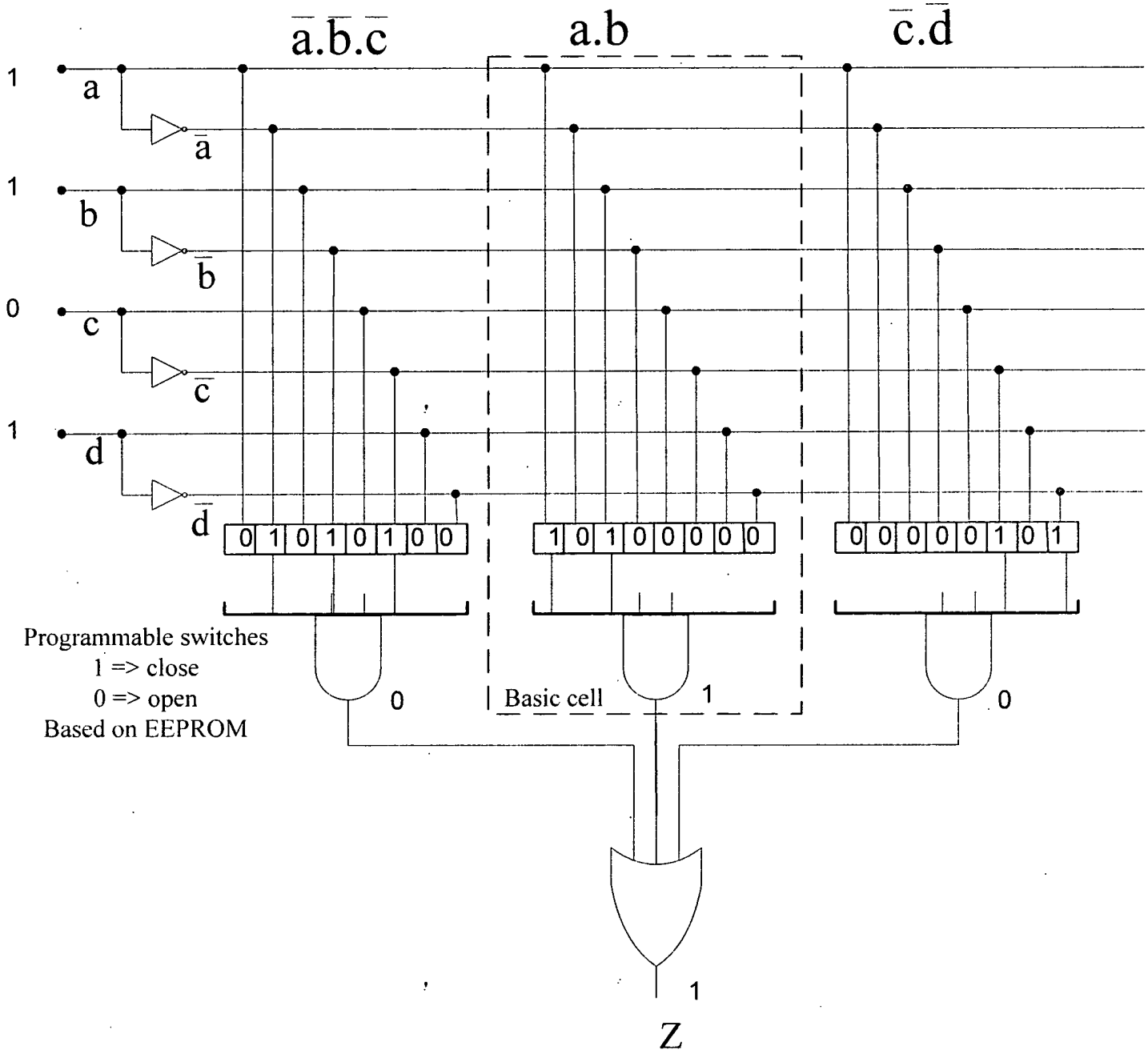


FIGURE 12

Example showing a simplified cell in a first solution of CPLD
device, based on PAL
(Like ALTERA MAX 7000)

PAL => one level of switches

$$Z = \bar{a}.\bar{b}.\bar{c} + a.b + \bar{c}.d$$



1. For inputs: $a = 1$; $b = 1$; $c = 0$; $d = 1$, $a.b$ is an active product term, so $Z = 1$
2. For inputs: $a = 1$; $b = 0$; $c = 0$; $d = 1$, no active product term, so $Z = 0$

FIGURE A

Example showing a simplified cell in a first solution of FPGA
device based on LUT
(Like ALTERA FLEX 10K)

$$Z = \bar{a}.\bar{b}.\bar{c} + a.b + \bar{c}.d$$

$$Z = a.b.c.d + a.b.c.\bar{d} + a.b.\bar{c}.d + a.b.\bar{c}.\bar{d} + a.\bar{b}.c.d + a.\bar{b}.c.\bar{d} + a.\bar{b}.\bar{c}.d + a.\bar{b}.\bar{c}.\bar{d}$$

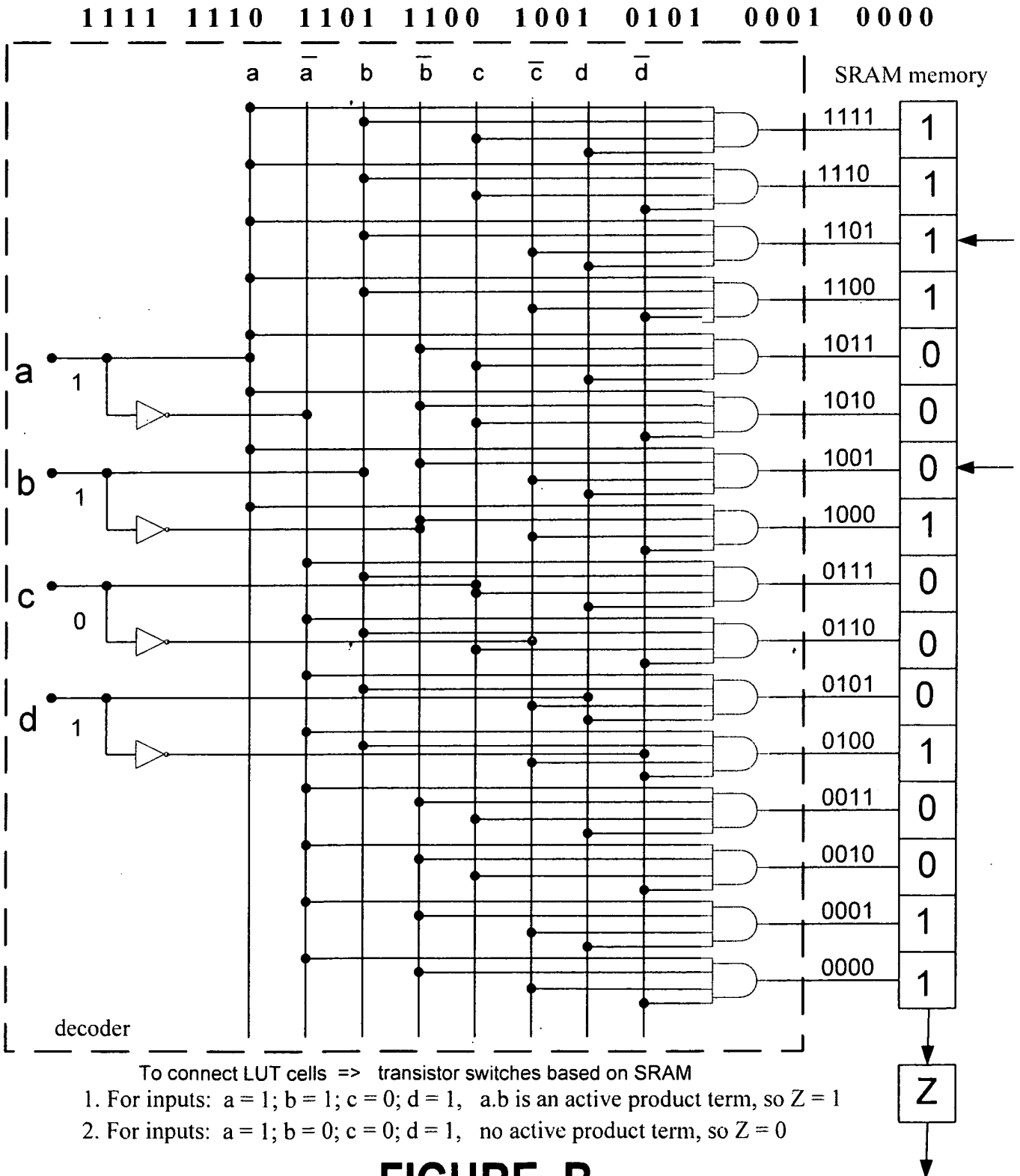
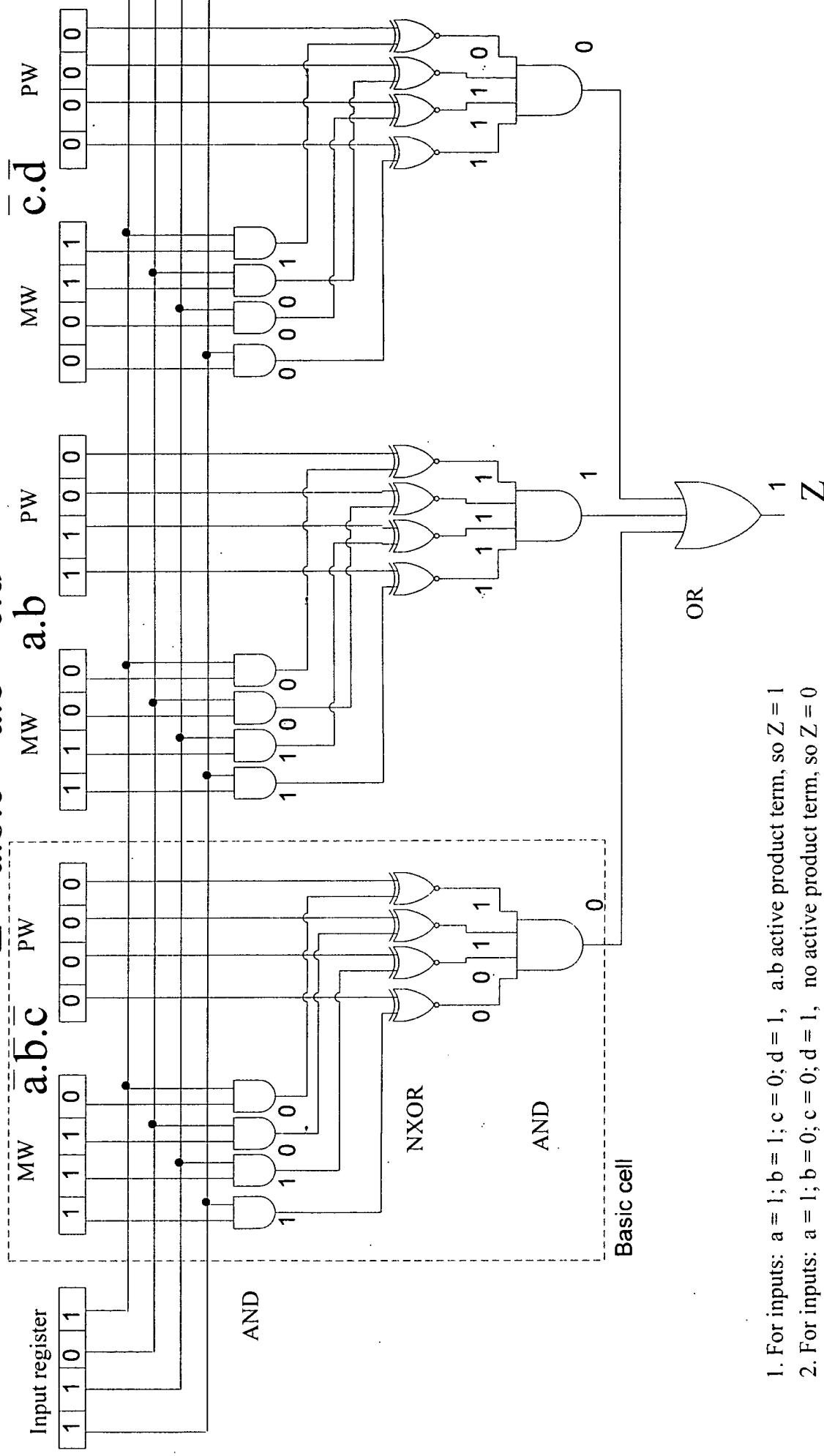


FIGURE B

A simplified hardware structure for the first proposed solution, considering the same logical equation

$$Z = a.b.c + a.b.\bar{c} + a.\bar{b}.c + a.\bar{b}.\bar{c}$$



1. For inputs: $a = 1; b = 1; c = 0; d = 1$, $a.b$ active product term, so $Z = 1$
2. For inputs: $a = 1; b = 0; c = 0; d = 1$, no active product term, so $Z = 0$

FIGURE C